REMARKS

The essentials of the invention process will be given to foster better grasp of the distinction between the invention process of reducing negative bias temperature instability (NBTI/NBTS) when fabricating a narrow channel width PMOSFET device compared to the methods disclosed by Kunikiyo and the newly cited reference of Bulat et al.

In producing PMOSFET devices, where negative bias temperature instability (NBTI) is a limiting factor insofar as the reliability of the PMOSFET is concerned, where the basic cause of NBTI remains unknown, where knobs sometimes used to reduce NBTI are very limited, where the use of fluorine is known to reduce NBTI when introduced through a BF_2 source/-drain self aligned implant or a flourine implant into the poly Si gate, and wherein the amount of fluorine dose is high and capable of only improving reduction of NBTI up to a certain limit, applicant has invented an improvement process for fabricating narrow channel width PMOSFET devices by improvement of reduction of negative bias temperature instability by the use of F_2 sidewall implantation.

This has unexpectedly been accomplished by:

a) forming a shallow trench isolation (STI) region in a substrate having a pad oxide and a nitride layer on its surface;

b) forming a gate on a gate oxide in said substrate;

c) forming a liner layer in said shallow trench isolation region and subjecting said liner layer to oxidation to form a STI liner oxidation layer;

d) implanting F_2 into side walls of said STI liner oxidation layer at a large tilted angle in sufficient amounts to affect reduction of negative bias temperature instability and enhance gate oxidation at the STI corner after a high density plasma fill of said STI F_2 implanted liner oxidation layer; and

e) filling the STI F_2 implanted structure from step d) with a high density plasma (HDP) fill to affect reduction of negative bias temperature instability.

Kunikiyo is only directed to making a semiconductor device whose element isolation structure is a STI structure having a bird's beak on its upper end, wherein silicon oxynitride film suppresses excessive growth of the bird's beak and prevents the bird's beak from forming of a depressed part, wherein reduction of the area of an active region caused by the bird's beak is suppressed without any depression part formed on the upper end of the STI structure.

Kunikiyo lacks applicant's step d) of implanting F_2 into sidewalls of the STI liner oxidation layer at a large tilted angle in sufficient amounts to affect reduction of negative bias instability after a high density plasma fill of said STI F_2 implanted liner oxidation layer.

This deficiency of Kunikiyo is not found in the teachings in the secondary reference of Bulat et al.

Bulat et al. is directed to a method of fabricating a semiconductor device structure comprising:

providing a body of silicon;

forming a groove in said body at a surface thereof;

forming layers of silicon oxide on the side walls and bottom of said groove;

introducing fluorine into said layers of silicon oxide; and

heating to activate said fluorine.

In actuality, Bulat et al. only implants fluorine into a silicon oxide layer 21 present in STI trenches and on the corresponding ridges.

By contrast, in the present invention, on the ridges, a nitride layer on a pad oxide is present, which performs the function of a mask. Consequently, there is no implantation performed into the ridges. This has the effect that, not only is negative bias temperature instability overcome, but the gate oxidation at the STI corner is also enhanced (as can be seen from FIG. 1 of the invention).

Column 3, lines 61-64 of Bulat et al. relates to the implant oxide to prevent channeling of ions along silicon grain boundaries; however, this implant oxide has nothing to do with the fluorine implantation because it is applied to exposed ridges, as can be seen in FIG. 5 of Bulat et al.

As such, even if the F_2 implantation taught in Bulat et al. were substituted into the fabrication process of Kunikiyo, applicant's fabrication process would not result. Neither would applicants' fabrication process be rendered obvious for the reason that applicant's process requires a nitride on a pad oxide, which performs the function of a nitride layer mask

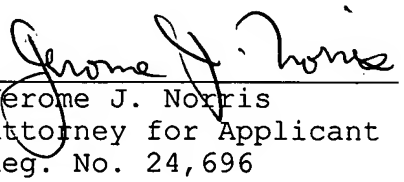
- and no implantation is performed into the ridges, as is clearly the case in Bulat et al.

From pages 8 and 9 of applicant's specification, it has been found that during formation of the PMOSFET at the poly Si/SiO_2 interface there is a threshold voltage shift ΔV_{th} and degradation of the device after a negative bias temperature stress, whereas under a plus bias temperature stress, the threshold voltage shift (ΔV_{th}) is negligibly small. The ΔV_{th} is given by a power law, $\Delta V_{th} \sim T^a$, with a equal to 1/3. By virtue of applicant's inclusion in its PMOS device of the outside layer on the pad oxide, wherein the nitride layer functions as a mask, there is affectation of reduction of negative bias temperature instability - and this is not taught in either Kunikiyo or Bulat et al. et al. alone or in combination.

The In re Aller, Woodruff Merck & Co., Ex parte Ishizaka, and In re Burckel decision shows that they are non-apropos to the facts at bar, given that neither of the references implant F_2 as does applicant from a PMOS device characterized by substrate pad oxide and a nitride layer, wherein the nitride layer functions as a mask - thereby preventing a threshold voltage shift ΔV_{th} and degradation of the device due to the avoidance of a negative bias temperature stress in accordance with the power law given on page 8 of applicant's specification.

It is respectfully requested that the foregoing be taken into consideration prior to taking this application up for examination on the merits.

Respectfully submitted,



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